

EXHIBIT 2
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April 29, 2023

VIA E-MAIL

Michael R. Rueckheim
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Re: Netlist, Inc. v. Micron Technology, Inc. et al, 22-cv-203-JRG-RSP (E.D. Tex.)

Dear Mr. Rueckheim:

We write regarding significant deficiencies that remain in Micron's document production, as detailed below. We reference Micron to the letter dated November 10, 2022 where Netlist expressly requested certain categories of documents for production. Micron has simply ignored those requests.

As explained below, the requested documents are relevant to Netlist's infringement claims because they are necessary to understanding the structure and function of the accused products. Micron was required to produce all of these documents by the P.R. 3-4 deadline, but failed to do so. Given the fast-approaching deadlines for the substantial of completion of document production and opening expert reports, please commit to remedying these deficiencies with Micron's production by May 5, 2023.

I. Micron's Production of Technical Documents Regarding The Accused HBM2, HBM2E, HBM3, and HBMnext Products Remains Deficient

Netlist has been seeking discovery related to the structure and operation of Micron's HBM products for several months. Netlist's November 10, 2022 discovery letter listed several categories of technical documents relevant to Micron's HBM products, including documents "related to the configuration, implementation, or operation of the control die (e.g., buffer die or logic die) in Micron Accused HBM Products" and the "configuration and interconnections of the die interconnects (e.g. TSVs) in Micron Accused HBM Products." 2022-11-10 Zhao Ltr. to Rueckheim at 11-12. These features are relevant to the asserted '060 and '160 patents. For example, claim 1 of the '060 patent is directed to a memory package with "die interconnects" in electrical communication with some, but not all, of the array dies in the memory package. '060, cl. 1 ("[T]he first die interconnect in electrical communication with

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the first group of array dies and not in electrical communication with the second group of at least one array die.”).

The manner of interconnection of the die interconnects in Micron’s HBM Products, *e.g.* how the TSVs are arranged, is plainly relevant to the asserted claims. Netlist’s September 8, 2022 preliminary infringement contentions make clear that the manner of die interconnection is a central aspect of Netlist’s infringement theory:

Exhibit E - Infringement of U.S. Patent 8,787,060

(1c) at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and	<p>The Accused Instrumentalities further comprise at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.</p> <p>For example, a first die interconnect may be in electrical communication with the first group of array dies (<i>e.g.</i>, (i) two or more of the bottom DRAM dies or (ii) a set of dies communicating through a same (first) data channel or data channels, such as dies 1 and 5 (colored in red), dies 2 and 6 (colored in green), dies 3 and 7 (colored in yellow), and dies 4 and 8 (colored in orange)) and not in electrical communication with the second group of at least one array die (<i>e.g.</i>, (i) at least one of the top DRAM dies or (ii) another set of dies communicating through a second data channel), and the second die interconnect may be in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies. On information and belief, this is achieved by coupling certain TSVs with active transceiver logic for only a subset of the dies. For example, some TSVs electrically interconnect only the first group of DRAM dies with the underlying control die (labeled as both a “buffer die” or “logic die” above) while some bypass these same first group of DRAM dies and electrically connect with the active transceiver logic of only the second group of DRAM dies. For instance, in one implementation, a first set of TSVs interconnect is in electrical communication with only dies 1 and 5 (colored in red), but not in electrical communication with dies 4 and 8 (colored in orange), dies 3 and 7 (colored in yellow), or dies 2 and 6 (colored in green) (each pair can be a second group of array dies). A second set of TSVs interconnect is in electrical communication with dies 4 and 8, for example, but are not in electrical communication with dies 1 and 5 (or with dies 2 and 6 or dies 3 and 7). As another example, some transceiver logic in certain array dies is disabled through programming steps. As an additional example, changes in metallization patterning, via patterning, via interconnection patterns, configuration and programming (including design-time, manufacturing-time, test-time, training-time, and run-time), or any other mechanism to create a physical or logical open circuit causes electrical signals to be received at a subset of array dies.</p>
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Netlist has repeatedly asked Micron to remedy these deficiencies in its document production. *See, e.g.*, 2023-03-08 Werner Ltr. to Rueckheim (noting Micron “has failed to produce technical documents” regarding its HBM products). Netlist also filed a motion to find Micron in violation of P.R. 3-4(a) when it became clear that Micron would continue to refuse to produce technical documents regarding its HBM products. Dkt. 49 at 1-2. However, to date Micron has only produced [REDACTED] as part of its P.R. 3-4 production. As summarized in the table below, many of these documents are publicly available, or materially identical to publicly available documents. These documents are insufficient to show the pattern of die interconnection in Micron’s HBM products, which, as explained above, is highly relevant to Netlist’s infringement theory for the ’060/’160 patents. Nor do those documents provide sufficient information on the buffer die layout or signaling protocols relevant to *e.g.*, whether the accused products feature a “control

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die . . . comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.” ’060, cl. 1; *see also* ’160, cl. 5; ’060, cl. 7 (“wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit” of the claimed “control die”).

Document	Bates
Publicly available datasheets cited in Netlist’s PICs (2)	MICNL203-00000697 (duplicative of MICNL203-00001188).
Confidential datasheets generally mirroring publicly available JEDEC specifications (2)	MICNL203-00000697 (duplicative of MICNL203-00001188)
Publicly available documents introducing the HBM products or packaging procedures (3)	MICNL203-00002557; MICNL203-00002688; MICNL203-00002738
Publicly available website captures or news blogs, which provide no details relevant to operation and function of the accused features (7)	MICNL203-00002634; MICNL203-00002700; MICNL203-00002745; MICNL203-00003661; MICNL203-00003674; MICNL203-00003690; MICNL203-00003701.

As detailed in Netlist’s Motion, Micron’s refusal to produce documents regarding its HBM products based on its belief that Netlist had not stated a cognizable infringement theory for the ’060/’160 patents is an improper basis to resist discovery. *See* Dkt. 49 at 6-7. In any event, Micron’s belief that Netlist has not stated a cognizable infringement theory is mistaken. On March 28, 2023, Judge Gilstrap denied Samsung’s motion for summary judgment of non-infringement of the ’060/’160 patents in the parallel Samsung case. *See Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-463-JRG (E.D. Tex.) (“*Samsung I*”), Dkt. 432 at 2. On April 20, Judge Gilstrap also denied Samsung’s Rule 50(a) motion for judgment as a matter of law on the same patents. And on April 21, the jury in *Samsung I* found the ’060/’160 patents infringed. Micron has no basis to continue resisting discovery into these products based on its belief that it does not infringe the ’060/’160 patents.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

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[REDACTED]

II. Micron's Production of Documents Relating to Testing, Evaluation, and Simulation Data and Other Relevant Documents Related to the Accused Products Is Deficient

Netlist's November 10, 2022 discovery letter listed several categories of documents relating to testing, evaluation, and simulation data related to the accused products that Micron has not produced.

For example, for Micron's DDR5 DIMMs, Netlist listed the following categories of documents, all of which are relevant to infringement of the '918 and '054 patents:

48. All studies, analyses, reports, or other documents in Micron's possession, control, or custody related to implementing the power management circuitry (including voltage regulation and monitoring circuitry) on the module board instead of on the motherboard in Micron Accused DDR5 DIMMs, including simulations performed by Micron and/or third parties.

52. Documents sufficient to fully describe all testing (and results of that testing) Micron did or commissioned others to do to ensure the proper implementation of power management circuitry on the module board in Micron Accused DDR5 DIMMs.

Likewise, Netlist requested testing and evaluation documents related to the signaling and load-reduction aspects of Micron's HBM products, which is relevant to infringement of the '060 and '160 patents:

68. Documents sufficient to fully describe the HBM layout, interconnections, and signaling in Micron Accused HBM Products, including, but not limited, to documents related to: . . . (4) how Micron Accused HBM Products electrically isolate or reduce the load presented by the die interconnects (e.g., TSVs). . . Such documents include, but are not limited to, circuit diagrams, design files, Source Code, application notes, specifications, datasheets, descriptions of operation principles, functional block diagrams, and presentations of the relevant integrated circuits and components.

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70. Documents sufficient to fully describe all testing (and results of that testing) Micron did or commissioned others to do to ensure proper communication of data, control, and address signals to the control die (e.g., buffer die or logic die) and the DRAM dies in Micron Accused HBM Products.

117. Studies and evaluations performed by Micron or third parties on whether TSVs for signals should be selectively connected to only selected drivers in a selected subset of DRAM chips or to be connected to all DRAM chips.

Similarly, Netlist requested testing and evaluation documents related to data buffer timing in the accused DDR4 LRDIMMs, which is relevant to infringement of the '339 and '506 patents:

23. All studies, analyses, reports, or other documents in Micron's possession, control, or custody related to the operation of data buffers in Micron Accused DDR4 LRDIMMs, including simulations performed by Micron and/or third parties.

27. Documents sufficient to fully describe all testing (and results of that testing) Micron did or commissioned others to do to ensure proper LRDIMM Data Buffer Read Timing in Micron Accused DDR4 LRDIMMs.

39. Documents sufficient to fully describe all testing (and results of that testing) Micron did or commissioned others to do to ensure proper timing of the enablement/disablement of write or read buffers in Micron Accused DDR4 LRDIMMs.

Id. at 6-8.

To date, Micron has not produced any current testing or evaluation documents for of the accused products. Netlist requests that by May 5, 2023 Micron commit to producing all testing and evaluation documents related to the patents-in-suit.

Micron also does not appear to have produced relevant documents in its possession, control or custody that it has received from its customers or suppliers as related to the accused features. Netlist's November 10, 2022 letter expressly requested that Micron produce such documents. *See, e.g., id.* at 6 (RFP #23 requesting Micron produce "All studies, analyses, reports, or other documents ***in Micron's possession, control, or custody*** related to the

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operation of data buffers in Micron Accused DDR4 LRDIMMs”), *id.* at 7 (RFP #48 requesting similar documents regarding structure and operation of Micron’s DDR5 DIMMs “in Micron’s possession, control, or custody”), *id.* at 11 (RFP #66 requesting similar documents regarding structure and operation of Micron’s HBM products “in Micron’s possession, control, or custody”). Please also commit to producing those documents by May 5, 2023.

III. Micron’s Production of Documents Relating to the Power Management and Voltage Regulation on Its DDR5 DIMMs Is Deficient

Netlist’s November 10, 2022 discovery letter also listed several categories of documents relating to the configuration of the power management circuitry in Micron’s DDR5 DIMMs. *See e.g.*, 2022-11-10 Zhao Ltr. to Rueckheim at 9 (“Documents sufficient to fully describe the power management and voltage regulation and monitoring in Micron Accused DDR5 DIMMs, including, but not limited to, documents related to how PMIC(s) in Micron Accused DDR5 DIMMs (1) produce regulated voltages; (2) monitor power input voltage; (3) respond to changes in power input voltage (e.g., an over-voltage or under-voltage condition); and (4) write information to non-volatile memory in response to changes in power input voltage.”). Netlist specified certain non-limiting types of documents responsive to this request, including, “circuit diagrams, design files, Source Code, application notes, specifications, datasheets, descriptions of operation principles, functional block diagrams, and presentations of the relevant integrated circuits and components.” *Id.*

Micron’s document production to date consists of [REDACTED] that are insufficient to describe the actual configuration of Micron’s DDR5 DIMMs, for example, how the regulated voltages output by the PMICs are coupled to the each component on Micron’s DDR5 DIMMs. This information is relevant to Netlist’s claims of infringement of the ’918 and ’054 patents, which require specific couplings between the voltage converters and other components on the module. *See, e.g.*, ’918 cl. 1 (“at least one circuit . . . coupled to both the second regulated voltage and the fourth regulated voltage”).

Netlist requests that by [REDACTED] in addition to any other relevant documents in its possession, control and custody, including those it received from its customers or suppliers and any testing, simulation or evaluation—whether performed by itself or others—in its possession, control or custody.

Sincerely,

/s/ Michael Tezyan
Michael Tezyan

cc: Counsel of Record (per agreed service emails)